UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,494	09/15/2003	Howard E. Rhodes	M4065.0087/P087-A	7413

24998 7590 11/12/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
BERARDESCA, PAUL M	
ART UNIT	PAPER NUMBER
2622	
MAIL DATE	DELIVERY MODE
11/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,494	RHODES, HOWARD E.	
	Examiner	Art Unit	
	PAUL BERARDESCA	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *80,81,84,85,88,89,93,94,97-99 and 102-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *80,84,88,93,97,98,102-104,106,107,109,111,113,115 and 117* is/are rejected.

7)☒ Claim(s) *81,85,89,94,99,105,108,110,112,114 and 116* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 8/29/2009 have been fully considered but they are not persuasive. Applicant argues that "There is no requirement that an applicant must address each and every point made by an Examiner in responding to his/her rejections set for in an office action…The Applicant's position is that he has not indicated that any feature of which the Examiner took official notice is considered prior art". While the examiner agrees that there is no requirement that an applicant must address each and every point made by an Examiner in responding to his/her rejections, an applicant must address an official notice statement with a proper traversal in the following response or else the facts officially noticed become admitted prior art. The following paragraph is taken from MPEP 2144.03 C with regards to traversing a finding of official notice:

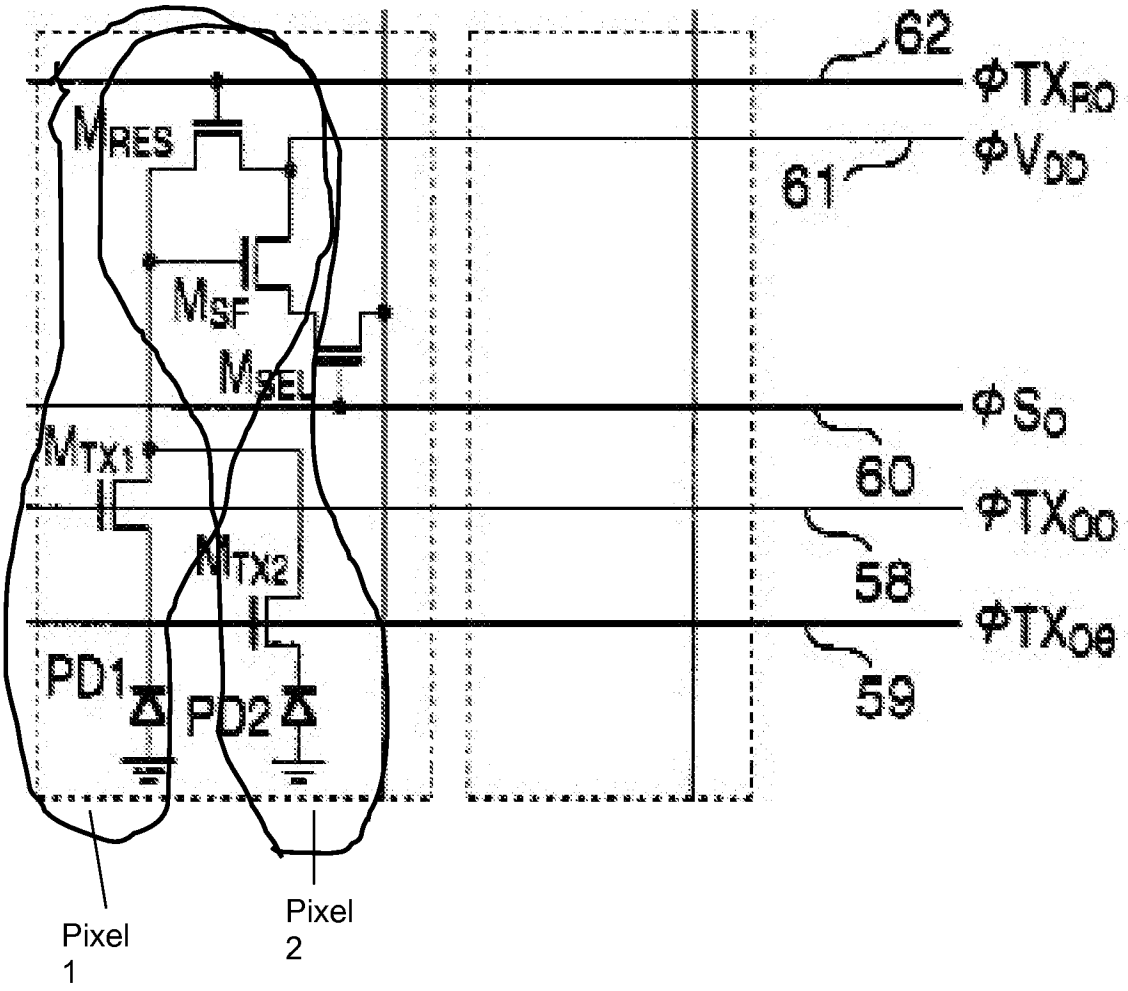
"To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art…A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate…If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate."

Applicant's arguments with respect to the minor informality objection of claim 102 have been fully considered but they are not persuasive. The current amendment does not address the previous minor informality objection.

Applicant's arguments, with respect to claim 80 have been fully considered but they are not persuasive. Applicant argues that "the two pixels of Hashimoto are not addressed by respective row select lines that connect the pixels to the shared column line for signal output, but instead have respective addressing transfer gate lines, which is different." The examiner cannot agree. Applicant has chosen one signal line in Hashimoto (62 in figure 10) and argues that this signal line and only this signal line can be interpreted as the row select line. Not only is the select line 62 not interpreted to be the claimed row select lines in the previous office action, but select lines 58 and 59 have all the characteristics of row select lines as claimed. Particularly, both of these lines, when made high, cause an amplified pixel signal to be output to a column line 57.

Applicant goes on to argue that "Transfer gates to not provide a connection for an output signal, but gate the photocharge generated at the photodiode to the pixels' floating diffusion regions". However, as shown in the timing diagram of figure 12, the row select signal ΦS_o, which Applicant states is the only row select line, is always on when either the select signal ΦTX_{oo} or ΦTX_{oe}, which the examiner argues are the row select lines. In other words, whenever, select lines 58 or 59 are turned on, an amplified charge from the first pixel (pixel containing PD1) or the second pixel (pixel containing

PD2) respectively, is provided to the column output line 57. The claim only requires that the row select lines, when activated, connect the associated one of the first and second pixels with the shared column. Figure 10 of Hashimoto is reproduced below to show what is interpreted as the first and second pixels.



Although pixels 1 and 2 share an amplifier, they have exclusive components, which makes them two separate entities. When TXoo is activated, the charge from PD1 is transferred to the gate of the source follower, where it is amplified and then

transferred from the output of the source follower (output of Pixel 1) directly to the column line 57 since transistor Msel is always turned on when TXoo is on. Similarly, when TXoe is activated, the charge from PD2 is transferred to the gate of the source follower, where it is amplified and then transferred from the output of the source follower (output of Pixel 2) directly to the column line 57. Therefore, 58 and 59 do in fact cause an amplified pixel signal to be output. For these reasons, select lines 58 and 59 read on claimed "first row select line" and "second row select line" respectively.

Applicant's arguments with respect to claim 84 have been fully considered but they are not persuasive (see examiner's response with respect to claim 80). In addition, as explained above, although the two adjacent pixels of Hashimoto share an amplifier, they do have exclusive components, and they are addressed at separate times, which make them separate entities. Therefore, it can be said that each of the two pixels has a node (the gate of the source follower transistor).

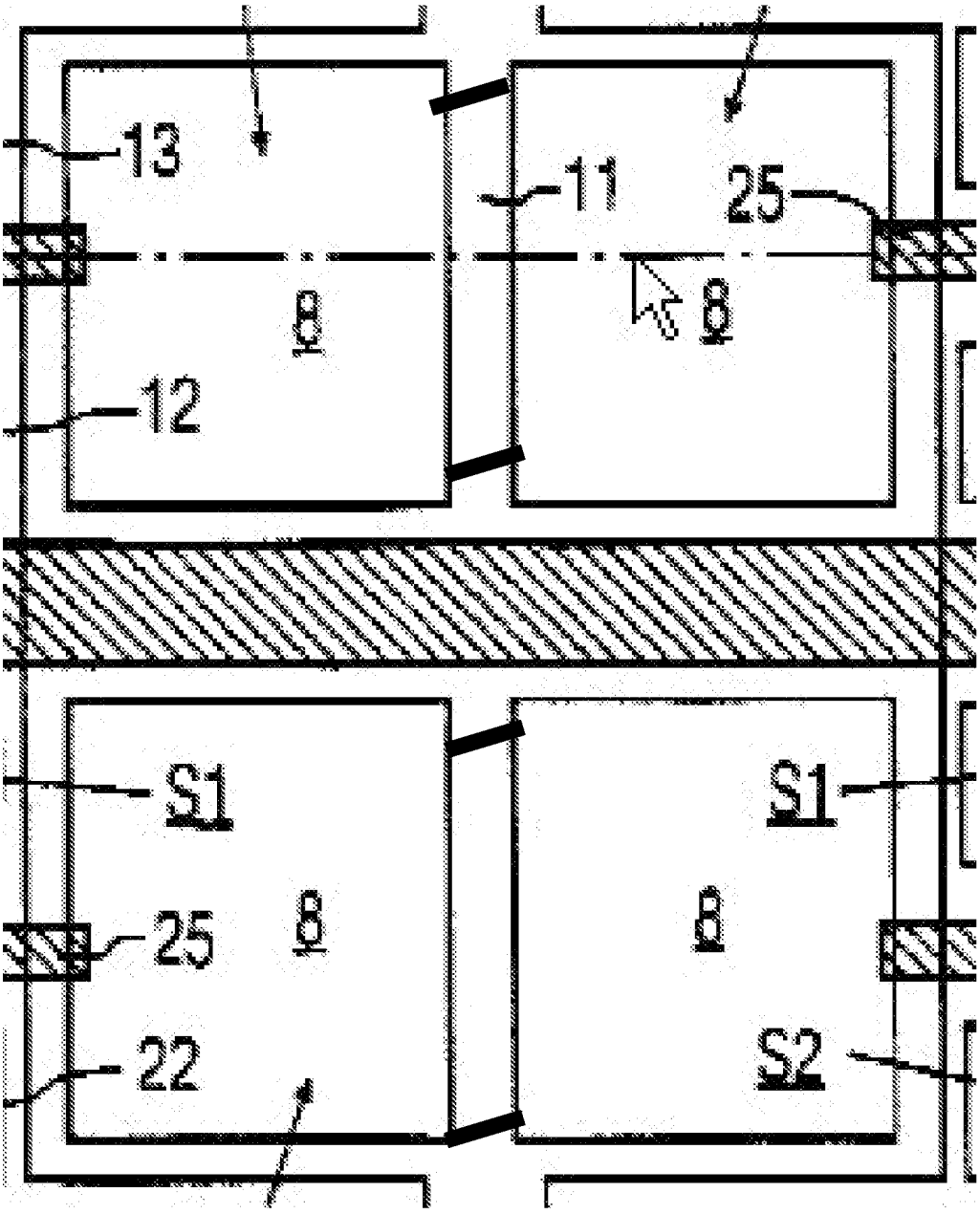
In addition, Applicant's deletion of the limitation "addressing the first pixel using the first row select line and then subsequently addressing the second pixel using the second row select line, the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row", has now made claim 84 indistinguishable from previously cited Bird (US Patent 5,721,422).

Applicant's arguments with respect to claims 88 and 93 have been fully considered but they are not persuasive (see examiner's response with respect to claim 80).

Applicant's arguments with respect to claims 102 and 106 have been fully considered but they are not persuasive (see examiner's response with respect to claim 80). In addition, claim 102 is not distinguishable from Bird and because of the amendment made to claim 106 on 3/11/2009, claim 106 is no longer distinguishable from Bird.

Applicant's arguments with respect to claim 97 have been fully considered but they are not persuasive. Applicant argues that "None of the cited references discloses this diagonal aspect of the connecting/shared active area in relation to the column line…In Bird, all active areas are at parallel and orthogonal angles relative to the column conductor (e.g., 11 of Fig. 5)." The examiner cannot agree. When the term "diagonal" is used as an adjective it defines a direction and not a shape. To say that an active area component is in a diagonal direction with respect to the column line does not limit the active area component to be in the shape of a diagonal line with respect to the column line, and therefore does not distinguish from any other active area component connecting the two pixels. Specifically, the active area can be interpreted to be in a diagonal direction anywhere. In other words, a diagonal line can be drawn anywhere from one pixel to the other across the shared active area and therefore it is "diagonal

where it connects the first pixel and the second pixel with respect to the column line" as broadly claimed. Shown below is a reproduced Bird figure 5 showing how the active area can be considered diagonal where it connects the two pixels.



Applicant's arguments with respect to claims 107 and 109 have been fully considered but they are not persuasive (see examiner's response with respect to claim 80).

Applicant's arguments with respect to claim 111 have been fully considered but they are not persuasive. Applicant argues that "No such pixel array is taught by Hashimoto, Brehmer, Bird, or Shinohara". The examiner cannot agree. Brehmer teaches this limitation. Not only is "an output line" broad enough to read on the final output line of the entire sensor array which is used by all the pixels, but the only limitation in the claim of the two pixels is that they are adjacent and not necessarily in the same row. Therefore the two pixels could be in the same column and share a column output as in Brehmer.

Applicant's arguments with respect to claim 113 have been fully considered but they are not persuasive. As explained above stating that an area connecting two pixels has a diagonal orientation with respect to a linear reference does not distinguish from any area connecting two pixels. Any part of the area connecting the two pixels in Hashimoto can be interpreted as "the shared active area" having a "diagonal orientation relative to the linear arrangement of the reset transistor".

Applicant's arguments with respect to claim 115 have been fully considered but they are not persuasive (see examiner's response with respect to claim 97).

Applicant's arguments with respect to claim 117 have been fully considered but they are not persuasive (see examiner's response with respect to claim 113).

Claim Objections

Claim 93 is objected to because of the following informalities: the limitations "the first row select lines" and "the second row select lines" have no antecedent basis. A first and second row select **line** (singular) is defined in the claim prior to this limitation, but plural first and second row select lines are not. Appropriate correction is required.

Claim 102 is objected to because of the following informalities: the limitations "the first row select lines" and "the second row select lines" have no antecedent basis. Specifically, a first row select line and second row select line, both singular, have been defined prior, but plural row select lines have not been defined. Appropriate correction is required.

Claim 117 is objected to because of the following informalities: the limitation "second source drain region" should be changed to second source/drain region. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 80, 84, 88, 93, 102-104, 106, 107, 109, 113, 115, and 117 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto et al. (US Patent 6,977,684 B1) hereinafter referenced as Hashimoto.

Regarding claim 80, Hashimoto discloses an arrangement of circuits in pixels each circuit shared by plurality of pixels, in image sensing apparatus.

In addition, Hashimoto discloses, **"providing a first row select line (58) and a shared column line (57) for a first pixel of an array, and providing a second row select line (59) and said shared column line (57) for a second pixel of said array adjacent said first pixel, wherein said first pixel and said second pixel are in a row of pixels and do not share a row select line and the first row select line (58) and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array"**, as exhibited in figures 5 and 10.

In addition, Hashimoto discloses, **"activating at least one of first row select line (58) and the second row select line (59) to connect the associated one of the first and second pixels with the shared column line (57)"**, as disclosed in column 11 lines 18-49 and exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses, **"outputting a signal over the shared column line (57) which is associated with the activated row select line by connecting at least one of the first pixel and the second pixel to said shared column line (57)"**, as disclosed in column 11 lines 18-30 and exhibited in figures 9-12.

Regarding claim 84, in addition, Hashimoto discloses focusing an image on an active pixel CMOS imager (optical system 21 focuses an image on CMOS sensor 22), the imager (22) comprising a pixel array, which reads on claimed, **"receiving an image on a pixel array comprising"**, as exhibited in figures 1, 2, and 10.

Hashimoto discloses, **"a first pixel and an adjacent second pixel in a row of pixels, a first row select line (58) and a shared column line (57) provided for the first pixel, a second row select line (59) and said shared column line (57) provided for the second pixel, each of said first and second pixels having a node for receiving photogenerated charges and a circuit for providing an output signal based on charges at said node to said shared column line (57) in response to an associated activated row select line"**, as exhibited in figures 9-12.

In addition, Hashimoto discloses, **"resetting a voltage level of said node associated with the first pixel to a predetermined voltage using a reset transistor"**, as disclosed in column 10 lines 6-15 and exhibited in figures 9 and 10.

In addition, Hashimoto discloses, **"activating the first row select line (58) to output a signal from the first pixel to the shared column line (57)"**, as disclosed in column 10 lines 16-33 and exhibited in figures 9-12.

Regarding claim 88, Hashimoto discloses, **"a plurality of pixels for generating charge associated with detected light, the plurality of pixels arranged in rows and columns of an array (fig. 2), each said row having interspersed odd and even pixels, wherein a odd pixel (PD1,Mtx1,Mres,Msf,Msel) of a row is addressed by an activated odd row select line (58) to provide an output signal on a column line (57) shared with an adjacent even pixel, and wherein the adjacent even pixel (PD2,Mtx2,Mres,Msf,Msel) of the row is addressed by an activated even row select line (59) to provide an output signal on the shared column line (57), wherein the even row select line (59) does not address the odd pixels and the odd row select line (58) does not address the even pixels"**, as exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses a column driver (71 and timing controller 25) to address pixels connected to the column lines (57), which reads on claimed, **"a column driver to access pixels connected to the shared column line"**, as exhibited in figures 1 and 10.

In addition, Hashimoto discloses a row driver (70) to address pixels through the odd row select lines (58) and the even row select lines (59) , which reads on claimed, **"a row driver to selectively activate the odd row select line and the even row select line"**, as exhibited in figure 10.

Regarding claim 93, Hashimoto discloses, **"providing a row select line (58) exclusively for first pixels (PD2,Mtx2,Mres,Msf,Msel) of a row of pixels and a second row select line (59) exclusively for second pixels of the row of pixels, wherein said first and second row select lines connect said first and second pixels to respective ones of a plurality of shared column lines (57), which are each shared by adjacent first and second pixels, when the first and second row select lines are respectively activated, wherein the first row select lines (58) do not address any second pixel and the second row select lines (59) do not address any first pixel"**, as exhibited in figures 9-12.

In addition, Hashimoto discloses addressing even pixels (PD2,Mtx2,Mres,Msf,Msel) in a row of an array of pixels using a row driver (70) coupled to an even row select line (59), which reads on claimed, **"addressing the first pixels using a row driver coupled to the first row select line"**, as exhibited in figure 10.

In addition, Hashimoto discloses providing a first output signal associated with light detected by the even pixels (PD2,Mtx2,Mres,Msf,Msel) to a plurality of column lines (57) coupled to the even pixels (PD2,Mtx2,Mres,Msf,Msel), which reads on claimed, **"providing a first output signal associated with light detected by the first pixels to**

the respective ones of the plurality of shared column lines by activating the first row select line (58)", as exhibited in figure 10.

In addition, Hashimoto discloses addressing odd pixels (PD1,Mtx1,Mres,Msf,Msel) using the row driver (70) coupled to the odd row select line (58), which reads on claimed, **"addressing the second pixels using the row driver coupled to the second row select line (59)"**, as exhibited in figure 10.

In addition, Hashimoto discloses providing a second output signal associated with light detected by the odd pixels (PD1,Mtx1,Mres,Msf,Msel) to the plurality of column lines (57) coupled to the odd pixels (PD1,Mtx1,Mres,Msf,Msel), which reads on claimed, **"providing a second output signal associated with light detected by the second pixels to the respective ones of the plurality of shared column lines (57) by activating the second row select line (59)"**, as exhibited in figure 10.

Regarding 102, Hashimoto discloses a pixel array comprising a row comprising a plurality of first pixels (PD1,Mtx1,Mres,Msf,Msel) and a plurality of second pixels (PD2,Mtx2,Mres,Msf,Msel), which reads on claimed, **"a pixel array comprising a row of first pixels and second pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses a respective column line (57) for each pair of first and second pixels of the row; and a reset line (62) connected to the plurality of first pixels, which reads on claimed, **"a first circuit (58,57) for the first pixels comprising a first row select line (58) for connecting the first pixels with respective ones of a plurality of shared column lines (57)"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"a second circuit (59,57) for the second pixels comprising a second row select line (59) for connecting the second pixels with said respective ones of said plurality of shared column lines (57), wherein the first row select lines (58) do not address the second pixels and the second row select lines (59) do not address the first pixels, each of the shared column lines (57) being associated with a first pixel and a second pixel"**, as exhibited in figures 9-12.

Regarding claim 103, Hashimoto discloses everything claimed as applied above (see claim 102), in addition, Hashimoto discloses wherein the plurality of first pixels are every other pixel in the row, which reads on claimed, **"wherein the plurality of first pixels are every other pixel in the row",** as exhibited in figures 2 and 10.

Regarding claim 104, Hashimoto discloses everything claimed as applied above (see claim 102), in addition, Hashimoto discloses wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line (57), which reads on claimed, **"wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line",** as exhibited in figure 10.

Regarding claim 106, Hashimoto discloses a row of pixels comprising a first plurality of pixels (PD1,Mtx1,Mres,Msf,Msel) and a second plurality of pixels

(PD2,Mtx2,Mres,Msf,Msel), a first address line (58) addressing only the first plurality of said pixels and a second address line (59) addressing only the second plurality of said pixels, which reads on claimed, **"a row of pixels comprising a first plurality of pixels and a second plurality of pixels"**, as exhibited in figures 2 and 10.

In addition Hashimoto discloses, **"a first address circuit (58,57) for the first plurality of said pixels and a second address circuit (59,57) for the second plurality of said pixels, said first address circuit comprising a first row select line (58) and a plurality of shared column lines (57), and said second address circuit comprising a second row select line (59) and said plurality of shared column lines (57), wherein the first row select lines (58) do not address the second plurality of pixels and the second row select lines (59) do not address the first plurality of pixels, each of said plurality of shared column lines (57) being connected to a respective first pixel of the first plurality of pixels and a respective second pixel of the second plurality of pixels by the first row select line (58) and the second row select line (59)"**, as exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses a reset line (62) connected to at least the first plurality of pixels or the second plurality of pixels, which reads on claimed, **"a reset line connected to at least the first plurality of pixels or the second plurality of pixels"**, as exhibited in figures 2 and 10.

Regarding claim 107, Hashimoto discloses, **"a row of a plurality of first pixels alternated with a plurality of second pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"a first row select line (58) dedicated to only said row and only the first pixels of said row, wherein said first row select line (58) controls a signal output switch (MTX1) for a plurality of first pixels of said row"**, as exhibited in figures 10 and 12.

In addition, Hashimoto discloses, **"a second row select line (59) dedicated to only said row and only the second pixels of said row, wherein said second row select line (59) controls a signal output switch (MTX) for a plurality of second pixels of said row"**, as exhibited in figures 10 and 12.

In addition, Hashimoto discloses, **"at least one common output line (57) shared by said row and a plurality of other rows of pixels, wherein said common output line is shared by at least a pair of adjacent first and second pixels of said row"**, as exhibited in figure 10.

Regarding claim 109, Hashimoto discloses, **"a row of pixels, including odd column pixels alternated with even column pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"an odd output selection circuit (MTX1) for connecting an odd column pixel of the row to a column output line (57), the odd output selection circuit being driven by an odd pixel selection signal line (58) common to only the odd columns of pixels of the row"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"an even output selection circuit (MTX2) for connecting an even column pixel of the row to the column output line (57), the even output selection circuit (MTX2) being driven by an even pixel selection**

signal line (59) common to only the even column pixels of the row", as exhibited in figure 10.

Regarding claim 113, Hashimoto discloses, **"a pixel array having pixels arranged in rows and columns"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"said pixel array comprising a first pixel and a second pixel formed in respectively adjacent columns and in conjunction with an active area spanning between a first photodetector of the first pixel and a second photodetector of the second pixel but no other photodetectors, said active area having the first associated photodetector and the second associated photodetector at opposite ends of said active area"**, as exhibited in figure 6.

In addition, Hashimoto discloses, **"a common output for charges (55) generated from the first photodetector and the second photodetector at a portion of said active area between said first and second photodetectors, the common output being coupled to a column line (61) shared by the first pixel and the second pixel, wherein the portion of said active area to which the common output is connected is configured diagonally with respect to an extending direction of said column line within the pixel array"**, as exhibited in figure 6. The Vdd line 61 reads on the claimed "column line" because according to claim 113 a column line is any signal line oriented in a column direction shared by a first and second pixel and coupled to a common output, both of which are characteristics of the Vdd line 61.

Regarding claim 115, Hashimoto discloses, **"a first pixel and a second pixel, the first pixel having a first photodetector (PD1) and the second pixel having a second photodetector (PD2) wherein the first photodetector shares an active area with the second photodetector and no other photodetector, said shared active area providing an output for said first and second photodetectors"**, as exhibited in figure 6.

In addition, Hashimoto discloses, **"a common readout line (57) for receiving a signal from said first and second photodetectors the active area shared by the first pixel and the second pixel, wherein the shared active area is oriented diagonally relative to an extending direction of the common readout line across the pixel array"**, as exhibited in figure 6.

Regarding claim 117, Hashimoto discloses, **"a first pixel and a second pixel, said first pixel having a first photodetector (PD1) and said second pixel having a second photodetector (PD2), wherein said first photodetector shares an active area with said second photodetector and no other photodetector and at least one of said first pixel and said second pixel further comprises a reset transistor (Mres, 63), said reset transistor comprising a gate, a first source/drain region, and a second source drain region linearly arranged, wherein said shared active area between the first and second photodetectors has a diagonal orientation relative to the linear arrangement of the reset transistor"**, as exhibited in figure 6.

Claim 111 is rejected under 35 U.S.C. 102(e) as being anticipated by Brehmer et al. (US Patent 6,130,423) hereinafter referenced as Brehmer.

Regarding claim 111, Brehmer discloses a method and apparatus for a CMOS image sensor with a distributed amplifier. In addition, Brehmer discloses, **"a first pixel comprising a first photodiode (620), a first source follower transistor (621) configured to provide a pixel output signal based on charges collected by the first photodiode (620), and a first pixel output selection switch (650) configured to connect the output signal of the first source follower transistor (621) to an output line"**, as exhibited in figure 6.

In addition, Brehmer discloses, **"a second pixel adjacent the first pixel (adjacent in the column) comprising a second photodiode (620), a second source follower transistor (621) configured to provide a pixel output signal based on charges collected by the second photodiode, and a second pixel output selection switch (650) configured to connect the output signal of the second source follower (621) transistor to the output line, wherein the output line is shared between the first pixel and the second pixel"**, as exhibited in figures 1 and 6.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 84, 97, and 98 are rejected under 35 U.S.C. 102(b) as being anticipated by Bird (US Patent 5,721,422).

Regarding claim 84, Bird discloses electronic devices having an array with shared column conductors. In addition, Bird discloses, **"receiving an image on a pixel array comprising a first pixel and an adjacent second pixel in a row of pixels, a first row select line (1) and a shared column line (11) provided for the first pixel, and a second row select line (2) and said shared column line (11) provided for the second pixel, each of said first and second pixels having a node for receiving photogenerated charges and a circuit for providing an output signal based on charges at said node to said shared column line (11) in response to an associated activated row select line"**, as disclosed in column 6 lines 13-58 and exhibited in figures 1 and 2.

In addition, Bird discloses, **"resetting a voltage level of said node associated with the first pixel to a predetermined voltage using a reset transistor (57,58)"**, as disclosed in column 6 lines 13-58 and exhibited in figures 1 and 2.

In addition, Bird discloses, **"activating the first row select line (1) to output a signal from the first pixel to the shared column line (11)"**, as disclosed in column 6 lines 13-58 and exhibited in figures 1 and 2.

Regarding claim 97, Bird discloses electronic devices having an array with shared column conductors. In addition, Bird discloses, **"a row comprising a first pixel (A pixel) and a second pixel (B pixel); the first and second pixels being joined by a common active area component"**, as exhibited in figures 5 and 7.

In addition, Bird discloses, **"a column line (11) connected with the first (A) and second (B) pixels at the common active area component, wherein said common active area component is diagonal where it connects the first pixel and the second pixel with respect to the column line (11)"**, as exhibited in figures 5 and 7.

In addition, Bird discloses, **"a first row select line (1) for connecting the first pixel (A) with the column line (11) to allow an output signal to be transferred from the first pixel to the column line (11)"**, as disclosed in column 6 lines 13-58 and exhibited in figures 1, 2, and 7.

In addition, Bird discloses, **"a second row select line (2) for connecting the second pixel (B) with the column line (11) to allow an output signal to be transferred from the second pixel (B) to the column line (11), Wherein the first row select line does not address the second pixel and the second row select line does not address the first pixel"**, as disclosed in column 6 lines 13-58 and exhibited in figures 1, 2, and 7.

Regarding claim 98, Bird discloses everything claimed as applied above (see claim 97), in addition, Bird discloses, **"wherein the row further comprises a plurality of first pixels (A) and a plurality of second pixels (B)"**, as exhibited in figure 7.

Allowable Subject Matter

Claims 81, 85, 89, 94, 99, and 105 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 81, Hashimoto discloses everything claimed as applied above (see claim 80), however, Hashimoto and Bird fail to disclose an S-shaped active area shared between the pixels.

Regarding claims 85, 89, 94, 99, 105, 108, 110, 112, 114, 116, they contain allowable subject matter for the same reasons as described above (see claim 81).

Conclusion

This is an RCE of applicant's earlier Application No. 10/661,494. All claims are drawn to the same invention claimed in the earlier application and could have been

finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL BERARDESCA whose telephone number is (571)270-3579. The examiner can normally be reached on Mon- Fri 8:30am-6:00pm EST (Alternate Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Berardesca
Examiner
Art Unit 2622

/P. B./
Examiner, Art Unit 2622
11/7/2009

/Sinh Tran/
Supervisory Patent Examiner, Art Unit 2622